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Search Results - Record(s) 1 through 9 of 9 returned.

☐ 1. Document ID: US 20020057446 A1

Using default format because multiple data bases are involved.

L7: Entry 1 of 9

File: PGPB

May 16, 2002

PGPUB-DOCUMENT-NUMBER: 20020057446

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020057446 A1

TITLE: MULTI- INSTRUCTION STREAM PROCESSOR

PUBLICATION-DATE: May 16, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
LONG, TIMOTHY MERRICK	LINDFIELD		AU	
GIBSON, IAN	COOGIE		AU	
AMIES, CHRISTOPHER	WILSTON		AU	

US-CL-CURRENT: 358/1.13; 358/1.15, 358/1.16, 382/307

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Ima
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☐ 2. Document ID: US 6674536 B2

L7: Entry 2 of 9

File: USPT

Jan 6, 2004

DOCUMENT-IDENTIFIER: US 6674536 B2

TITLE: Multi-instruction stream processor

Application Filing Date (1):

19980218

Detailed Description Paragraph Table (1):

TABLE 1 Register Description

NAME	TYPE	DESCRIPTION
External Interface Controller		
Registers eic_cfg	Config2	Configuration
eic_stat	Status	Status
eic_err_int	Interrupt	Interrupt
Error and Interrupt Status eic_err_int_en	Config2	Error and Interrupt Enable
eic_test	Config2	Test modes
eic_gen_pob	Config2	Generic bus programmable output bits
eic_high_addr	Config1	Dual address cycle offset
eic_wtlb_v	Control2	Virtual address and operation bits for TLB Invalidate/Write
eic_wtlb_p	Config2	Physical address and control bits for TLB Write
eic_mmu_v	Status	Most recent MMU virtual address translated, and current LRU location.
eic_mmu_v	Status	Most recent page table physical address fetched by MMU.
eic_ip_addr	Status	Physical address for most recent IBus access to the PCI Bus.
eic_rp_addr	Status	Physical address for most recent RBus access to the PCI Bus.
eic_ig_addr	Status	Address for most recent IBus access to the Generic Bus.
eic_rg_data	Status	Address for most recent RBus access to the Generic Bus.
Local Memory Controller		
Registers lmi_cfg	Control2	General configuration register
lmi_sts	Status	General status

register lmi_err_int Interrupt Error and interrupt status register lmi_err_int_en
 Control2 Error and interrupt enable register lmi_dcfg Control2 DRAM configuration
 register lmi_mode Control2 SDRAM mode register Peripheral Interface Controller Registers
 pic_cfg Config2 Configuration pic_stat Status Status pic_err_int Interrupt
 Interrupt/Error Status pic_err_int_en Config2 Interrupt/Error Enable pic_abus_cfg
 Control2 Configuration and control for ABus pic_abus_addr Config1 Start address for ABus
 transfer pic_cent_cfg Control2 Configuration and control for Centronics pic_cent_dir
 Config2 Centronics pin direct control register pic_reverse_cfg Control2 Configuration and
 control for reverse (input) data transfers pic_timer0 Config1 Initial data timer value
 pic_timer1 Config1 Subsequent data timer value Miscellaneous Module Registers mm_cfg
 Config2 Configuration Register mm_stat Status Status Register mm_err_int Interrupt Error
 and Interrupt Register mm_err_int_en Config2 Error and Interrupt Masks mm_gefg Config2
 Global Configuration Register mm_diag Config Diagnostic Configuration Register mm_grst
 Config Global Reset Register mm_gerr Config2 Global Error Register mm_gexp Config2 Global
 Exception Register mm_gint Config2 Global Interrupt Register mm_active Status Global
 Active signals Instruction Controller Registers ic_cfg Config2 Configuration Register
 ic_stat Status/ Status Register Interrupt ic_err_int Interrupt Error and Interrupt
 Register (write to clear error and interrupt) ic_err_int_en Config2 Error and Interrupt
 Enable Register ic_ipa Controll1 A stream Instruction Pointer ic_tda Config1 A stream Todo
 Register ic_fna Controll1 A stream Finished Register ic_inta Config1 A stream Interrupt
 Register ic_loa Status A stream Last Overlapped Instruction Sequence number ic_ipb
 Controll1 B stream Instruction Pointer ic_tdb Config1 B stream Todo Register ic_fnb
 Controll1 B stream Finished Register ic_intb Config1 B stream Interrupt Register ic_lob
 Status B stream Last Overlapped Instruction Sequence number ic_sema Status A stream
 Semaphore ic_semb Status B stream Semaphore Data Cache Controller Registers dcc_cfg1
 Config2 DCC configuration 1 register dcc_stat Status state machine status bits
 dcc_err_int Status DCC error status register dcc_err_int_en Controll1 DCC error interrupt
 enable bits dcc_cfg2 Control2 DCC configuration 2 register dcc_addr Config1 Base address
 register for special address modes. dcc_lv0 Controll1 "valid" bit status for lines 0 to 31
 dcc_lv1 Controll1 "valid" bit status for lines 32 to 63 dcc_lv2 Controll1 "valid" bit
 status for lines 64 to 95 dcc_lv3 Controll1 "valid" bit status for lines 96 to 127
 dcc_raddrb Status Operand Organizer B request address dcc_raddr Status Operand Organizer
 C request address dcc_test Controll1 DCC test register Pixel Organizer Registers po_cfg
 Config2 Configuration Register po_stat Status Status Register po_err_int Interrupt
 Error/Interrupt Status Register po_err_int_en Config2 Error/Interrupt Enable Register
 po_dmr Config2 Data Manipulation Register po_subst Config2 Substitution Value Register
 po_cdp Status Current Data Pointer po_len Controll1 Length Register po_said Controll1 Start
 Address or Immediate Data po_idr Control2 Image Dimensions Register po_muv_valid Control2
 MUV valid bits po_muv Config1 Ease address of MUV RAM Operand Organizer B Registers
 oob_cfg Config2 Configuration Register oob_stat Status Status Register oob_err_int
 Interrupt Error/Interrupt Register oob_err_int_en Config2 Error/Interrupt Enable Register
 oob_dmr Config2 Data Manipulation Register oob_subst Config2 Substitution Value Register
 oob_cdp Status Current Data Pointer oob_len Controll1 Input Length Register oob_said
 Controll1 Operand Start Address oob_tile Controll1 Tiling length/offset Register Operand
 Organizer C Registers ooc_cfg Config2 Configuration Register ooc_stat Status Status
 Register ooc_err_int Interrupt Error/Interrupt Register ooc_err_int_en Config2
 Error/Interrupt Enable Register ooc_dmr Config2 Data Manipulation Register ooc_subst
 Config2 Substitution Value Register ooc_cdp Status Current Data Pointer ooc_len Controll1
 Input Length Register ooc_said Controll1 Operand Start Address ooc_tile Controll1 Tiling
 length/offset Register JPEG Coder Register jc_cfg Config2 configuration jc_stat Status
 status jc_err_int Interrupt error and interrupt status register jc_err_int_en Config2
 error and interrupt enable register jc_rsi Config1 restart interval jc_decode Control2
 decode of current instruction jc_res Controll1 residual value jc_table_sel Control2 table
 selection from decoded instruction Main Data Path Register mdp_cfg Config2 configuration
 mdp_stat Status status mdp_err_int Interrupt error/interrupt mdp_err_int_en Config2
 error/interrupt enable mdp_test Config2 test modes mdp_op1 Control2 current operation 1
 mdp_op2 Control2 current operation 2 mdp_por Controll1 offset for plus operator mdp_bi
 Controll1 blend start/offset to index table entry mdp_bm Controll1 blend end or number of
 rows and columns in matrix, binary places, and number of levels in halftoning mdp_len
 Controll1 Length of blend to produce Result Organizer Register ro_cfg Config2
 Configuration Register ro_stat Status Status Register ro_err_int Interrupt
 Error/Interrupt Register ro_err_int_en Config2 Error/Interrupt Enable Register ro_dmr
 Config2 Data Manipulation Register ro_subst Config1 Substitution Value Register ro_cdp

Status Current Data Pointer ro_len Status Output Length Register ro_sa Config1 Start Address ro_idr Config1 Image Dimensions Register ro_vbase Config1 co-processor Virtual Base Address ro_cut Config1 Output Cut Register ro_lmt Config1 Output Length Limit PCIBus Configuration Space alias A read only copy of PCI configuration space registers 0x0 to 0xD and 0xF. pci_external_cfg Status 32-bit field downloaded at reset from an external serial ROM. Has no influence on coprocessor operation. Input Interface Switch Registers iis_cfg Config2 Configuration Register iis_stat Status Status Register iis_err_int Interrupt Interrupt/Error Status Register iis_err_int_en Config2 Interrupt/Error Enable Register iis_ic_addr Status Input address from IC iis_doc_addr Status Input address from DCC iis_po_addr Status Input address from PO iis_burst Status Burst Length from PO, DCC & IC iis_base_addr Config1 Base address of co-processor memory object in host memory map. iis_test Config1 Test mode register

Current US Original Classification (1):

358/1.15

Current US Cross Reference Classification (1):

358/1.9

Full	Title	Citation	Front	Review	Classification	Date	Reference	Searches	Attachments	Claims	KMIC	Draw Desc	Ima
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☐ 3. Document ID: US 6246396 B1

L7: Entry 3 of 9

File: USPT

Jun 12, 2001

DOCUMENT-IDENTIFIER: US 6246396 B1

TITLE: Cached color conversion method and apparatus

Application Filing Date (1):

19980218

Detailed Description Paragraph Table (2):

TABLE 1 Register Description NAME TYPE DESCRIPTION External Interface Controller Registers eic_cfg Config2 Configuration eic_stat Status Status eic_err_int Interrupt Error and Interrupt Status eic_err_int_en Config2 Error and Interrupt Enable eic_test Config2 Test modes eic_gen_pob Config2 Generic bus programmable output bits eic_high_addr Config1 Dual address cycle offset eic_wtlb_v Control2 Virtual address and operation bits for TLB Invalidate/Write eic_wtlb_p Config2 Physical address and control bits for TLB Write eic_mmu_v Status Most recent MMU virtual address translated, and current LRU location. eic_mmu_v Status Most recent page table physical address fetched by MMU. eic_ip_addr Status Physical address for most recent IBus access to the PCI Bus. eic_rp_addr Status Physical address for most recent RBus access to the PCI Bus. eic_ig_addr Status Address for most recent IBus access to the Generic Bus. eic_rg_data Status Address for most recent RBus access to the Generic Bus. Local Memory Controller Registers lmi_cfg Control2 General configuration register lmi_sts Status General status register lmi_err_int Interrupt Error and interrupt status register lmi_err_int_en Control2 Error and interrupt enable register lmi_dcfg Control2 DRAM configuration register lmi_mode Control2 SDRAM mode register Peripheral Interface Controller Registers pic_cfg Config2 Configuration pic_stat Status Status pic_err_int Interrupt Interrupt/Error Status pic_err_int_en Config2 Interrupt/Error Enable pic_abus_cfg Control2 Configuration and control for ABus pic_abus_addr Config1 Start address for ABus transfer pic_cent_cfg Control2 Configuration and control for Centronics pic_cent_dir Config2 Centronics pin direct control register pic_reverse_cfg Control2 Configuration and control for reverse (input) data transfers pic_timer0 Config1 Initial data timer value pic_timer1 Config1 Subsequent data timer value Miscellaneous Module Registers mm_cfg Config2 Configuration Register mm_stat Status Status Register mm_err_int Interrupt Error and Interrupt Register mm_err_int_en Config2 Error and Interrupt Masks mm_gefg Config2 Global Configuration Register mm_diag Config Diagnostic Configuration Register mm_grst

Config Global Reset Register mm_gerr Config2 Global Error Register mm_gexp Config2 Global Exception Register mm_gint Config2 Global Interrupt Register mm_active Status Global Active signals Instruction Controller Registers ic_cfg Config2 Configuration Register ic_stat Status/ Status Register Interrupt ic_err_int Interrupt Error and Interrupt Register (write to clear error and interrupt) ic_err_int_en Config2 Error and Interrupt Enable Register ici_ipa Controll A stream Instruction Pointer ic_tda Config1 A stream Todo Register ic_fna Controll A stream Finished Register ic_inta Config1 A stream Interrupt Register ic_loa Status A stream Last Overlapped Instruction Sequence number ic_ipb Controll B stream Instruction Pointer ic_tdb Config1 B stream Todo Register ic_fnb Controll B stream Finished Register ic_intb Config1 B stream Interrupt Register ic_lob Status B stream Last Overlapped Instruction Sequence number ic_sema Status A stream Semaphore ic_semb Status B stream Semaphore Data Cache Controller Registers dcc_cfg1 Config2 DCC configuration 1 register dcc_stat Status state machine status bits dcc_err_int Status DCC error status register dcc_err_int_en Controll DCC error interrupt enable bits dcc_cfg2 Control2 DCC configuration 2 register dcc_addr Config1 Base address register for special address modes. dcc_lv0 Controll "valid" bit status for lines 0 to 31 dcc_lv1 Controll "valid" bit status for lines 32 to 63 dcc_lv2 Controll "valid" bit status for lines 64 to 95 dcc_lv3 Controll "valid" bit status for lines 96 to 127 dcc_raddrb Status Operand Organizer B request address dcc_raddrc Status Operand Organizer C request address dcc_test Controll DCC test register Pixel Organizer Registers po_cfg Config2 Configuration Register po_stat Status Status Register po_err_int Interrupt Error/Interrupt Status Register po_err_int_en Config2 Error/Interrupt Enable Register po_dmr Config2 Data Manipulation Register po_subst Config2 Substitution Value Register po_cdp Status Current Data Pointer po_len Controll Length Register po_said Controll Start Address or Immediate Data po_idr Control2 Image Dimensions Register po_muv_valid Control2 MUV valid bits po_muv Config1 Base address of MUV RAM Operand Organizer B Registers oob_cfg Config2 Configuration Register oob_stat Status Status Register oob_err_int Interrupt Error/Interrupt Register oob_err_int_en Config2 Error/Interrupt Enable Register oob_dmr Config2 Data Manipulation Register oob_subst Config2 Substitution Value Register oob_cdp Status Current Data Pointer oob_len Controll Input Length Register oob_said Controll Operand Start Address oob_tile Controll Tiling length/offset Register Operand Organizer C Registers ooc_cfg Config2 Configuration Register ooc_stat Status Status Register ooc_err_int Interrupt Error/Interrupt Register ooc_err_int_en Config2 Error/Interrupt Enable Register ooc_dmr Config2 Data Manipulation Register ooc_subst Config2 Substitution Value Register ooc_cdp Status Current Data Pointer ooc_len Controll Input Length Register ooc_said Controll Operand Start Address ooc_tile Controll Tiling length/offset Register JPEG Coder Register jc_cfg Config2 configuration jc_stat Status status jc_err_int Interrupt error and interrupt status register jc_err_int_en Config2 error and interrupt enable register jc_rsi Config1 restart interval jc_decode Control2 decode of current instruction jc_res Controll residual value jc_table_sel Control2 table selection from decoded instruction Main Data Path Register mdp_cfg Config2 configuration mdp_stat Status status mdp_err_int Interrupt error/interrupt mdp_err_int_en Config2 error/interrupt enable mdp_test Config2 test modes mdp_op1 Control2 current operation 1 mdp_op2 Control2 current operation 2 mdp_por Controll offset for plus operator mdp_bi Controll blend start/offset to index table entry mdp_bm Controll blend end or number of rows and columns in matrix, binary places, and number of levels in halftoning mdp_len Controll Length of blend to produce Result Organizer Register ro_cfg Config2 Configuration Register ro_stat Status Status Register ro_err_int Interrupt Error/Interrupt Register ro_err_int_en Config2 Error/Interrupt Enable Register ro_dmr Config2 Data Manipulation Register ro_subst Config1 Substitution Value Register ro_cdp Status Current Data Pointer ro_len Status Output Length Register ro_sa Config1 Start Address ro_idr Config1 Image Dimensions Register ro_vbase Config1 co-processor Virtual Base Address ro_cut Config1 Output Cut Register ro_lmt Config1 Output Length Limit PCIBus Configuration Space alias A read only copy of PCI configuration space registers 0x0 to 0xD and 0xF. pci_external_cfg Status 32-bit field downloaded at reset from an external serial ROM. Has no influence on coprocessor operation. Input Interface Switch Registers iis_cfg Config2 Configuration Register iis_stat Status Status Register iis_err_int Interrupt Interrupt/Error Status Register iis_err_int_en Config2 Interrupt/Error Enable Register iis_ic_addr Status Input address from IC iis_doc_addr Status Input address from DCC iis_po_addr Status Input address from PO iis_burst Status Burst Length from PO, DCC & IC iis_base_addr Config1 Base address of co-processor memory object in host memory map. iis_test Config1 Test mode register

Current US Cross Reference Classification (4):
358/523

Current US Cross Reference Classification (5):
358/524

Current US Cross Reference Classification (6):
358/525

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Ima
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☒ 4. Document ID: US 5875287 A

L7: Entry 4 of 9

File: USPT

Feb 23, 1999

DOCUMENT-IDENTIFIER: US 5875287 A
TITLE: Banding noise reduction for clustered-dot dither

Application Filing Date (1):
19960226

Detailed Description Text (14):

To understand the way in which we suppress this effect, first consider the cluster-row spacing d in FIG. 4. We have found that we can suppress the banding effect if we offset successive clusters in the dither matrices by a fraction of that cluster-row spacing, as FIG. 5 illustrates. In FIG. 5, each successive column of matrix "tiles" is offset in the direction transverse to the scan direction by one-half the cluster-row spacing. (A column will be understood to extend in the direction transverse to the scan direction.) The fraction one-half is not required for application of this method, but it is a fraction that we have employed successfully. Although non-uniform scan spacing still distorts individual clusters, as clusters 64 suggest, the banding suppression that we have discovered appears to result from the fact that staggering the matrices tends to break up the bands of distorted clusters so that the eye is not nearly as sensitive to the distorted clusters' occurrence.

Detailed Description Text (20):

Alternatively, the stored matrix can be a submatrix of D' that yields the same cluster pattern even though it tiles the display in the conventional manner. For example, if the underlying conventional dither matrix of FIG. 3 is an $M \times N$ matrix that, as is typical, spans two cluster rows, one can store a matrix of $M \times 4N$ having the pattern that FIG. 6 suggests in order to achieve an offset of one-half of a cluster row. The resultant pattern follows the present invention's teachings, yet one can tile the display with the stored matrix in the conventional manner.

Current US Original Classification (1):
358/1.2

Current US Cross Reference Classification (1):
358/1.9

Current US Cross Reference Classification (2):
358/3.26

Current US Cross Reference Classification (3):
358/535

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	Ima
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☐ 5. Document ID: US 5781308 A

L7: Entry 5 of 9

File: USPT

Jul 14, 1998

DOCUMENT-IDENTIFIER: US 5781308 A

TITLE: High speed system for threshold matrix alignment and tiling, during creation of a binary half-tone image

Application Filing Date (1):
19960304Detailed Description Text (46):

Note that when the threshold matrix is tiled to coincide with the destination image resolution, there may be an offset in the ending bytes (if each threshold row is not an integer sub-multiple of the destination image). In such a case, the threshold matrix byte values at the end of a row in SRAM are "filled in" to assure a concurrent ending of both the threshold matrix row and the destination image. For example, during clock cycle 4, bytes A and B are used to fill in the word which is entered into pipeline register 222.

Current US Original Classification (1):
358/451Current US Cross Reference Classification (1):
358/3.23Current US Cross Reference Classification (2):
358/528

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	Ima
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☐ 6. Document ID: US 5778158 A

L7: Entry 6 of 9

File: USPT

Jul 7, 1998

DOCUMENT-IDENTIFIER: US 5778158 A

TITLE: High speed system for image scaling

Application Filing Date (1):
19960304Detailed Description Text (45):

Note that when the threshold matrix is tiled to coincide with the destination image resolution, there may be an offset in the ending bytes (if each threshold row is not an integer sub-multiple of the destination image). In such a case, the threshold matrix byte values at the end of a row in SRAM are "filled in" to assure a concurrent ending of both the threshold matrix row and the destination image. For example, during clock cycle 4, bytes A and B are used to fill in the word which is entered into pipeline register 222.

Current US Original Classification (1):
358/1.2Current US Cross Reference Classification (1):

358/1.1

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMIC	Draw Desc	Ima
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☐ 7. Document ID: US 5771105 A

L7: Entry 7 of 9

File: USPT

Jun 23, 1998

DOCUMENT-IDENTIFIER: US 5771105 A

TITLE: High speed system for grey level image scaling, threshold matrix alignment and tiling, and creation of a binary half-tone image

Application Filing Date (1):19960304Detailed Description Text (44):

Note that when the threshold matrix is tiled to coincide with the destination image resolution, there may be an offset in the ending bytes (if each threshold row is not an integer sub-multiple of the destination image). In such a case, the threshold matrix byte values at the end of a row in SRAM are "filled in" to assure a concurrent ending of both the threshold matrix row and the destination image. For example, during clock cycle 4, bytes A and B are used to fill in the word which is entered into pipeline register 222.

Current US Original Classification (1):358/2.99

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMIC	Draw Desc	Ima
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☐ 8. Document ID: US 5548689 A

L7: Entry 8 of 9

File: USPT

Aug 20, 1996

DOCUMENT-IDENTIFIER: US 5548689 A

TITLE: Method to convert bitmaps to monochrome data

Application Filing Date (1):19940503Detailed Description Text (20):

This dithering process begins with the selection of the correct dithering matrix for the first element 200 from the gray scale value array, as shown in box 74 as shown in FIG. 2C. Once the correct dither pattern matrix has been selected, the Y.sub.n position within the output image dither pattern tile for the particular output position bits to be dithered is determined as shown in box 76 so that the same Y.sub.DN position line within the dither pattern matrix can be selected. In a like manner, as shown in box 78, the X.sub.N position, or the bit offset within the destination bit map dithering tile for the first output position bit to be dithered is calculated and the selected Y.sub.DN row of the dithering pattern matrix is rotated, in box 80, to match the X.sub.DN position of the first output position bit from dithering matrix to the X.sub.N position of the first output bit in the destination dithering tile.

Current US Original Classification (1):358/1.9

Current US Cross Reference Classification (1):358/1.15

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KVMC	Draw Desc	Ima
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☐ 9. Document ID: US 5457772 A

L7: Entry 9 of 9

File: USPT

Oct 10, 1995

DOCUMENT-IDENTIFIER: US 5457772 A

TITLE: Method to convert bitmaps to monochrome data

Application Filing Date (1):19921013Detailed Description Text (31):

The dithering process begins with the selection of the correct dither pattern matrix for the first element 200 from the gray scale value array as shown in box 74. Once the correct dither pattern matrix has been selected, the Y position within the output image dither pattern tile for the particular output position bits to be dithered is calculated as shown in box 76 so that the same Y position row within the dither pattern matrix can be selected. In a like manner, as shown in box 78, the X position, or the bit offset within the destination bit map dithering tile for the first output position bit to be dithered is calculated and the selected Y row of the dithering pattern matrix is rotated, in box 80, to match the X position of the first output position bit from dithering matrix to the X position of the first output bit in the destination dithering tile.

Current US Original Classification (1):358/1.9

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KVMC	Draw Desc	Ima
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